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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,631	WORRELL, FRANK	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,442,642 to Brooks ("Brooks") and AMBA Specification Revision 2.0 ("AMBA").

3. In reference to Claim 1, Brooks discloses a bus comprising: a master interface (See 'BRIDGE' in Figures 1 and 5) connectable to a master device external to said bus (See 'HIGH-PERFORMANCE ARM PROCESSOR' in Figure 1) and configured to receive an early command signal from said master device at a first clock edge of a system clock (See Column 3 Line 15 – Column 4 Line 13) and present a bus wait signal to said master device proximate a second clock edge of said system clock (See Column

4 Table 1 'HREADY'); a slave interface (See 'BRIDGE' in Figures 1 and 5) connectable to a slave device external to said bus (See Figures 1 and 6) and configured to present a command signal to said slave device a delay after said first clock edge (See Column 3 Line 15 – Column 4 Line 13) and receive a slave wait signal from said slave device (See Column 7 Table 3 'BWAIT'); and a control logic configured to register said early command signal with said system clock to generate said command signal (See Column 3 Line 15 – Column 4 Line 13) and convert said slave wait signal into said bus wait signal (See Column 3 Line 15 – Column 4 Line 13).

4. Claims 13 and 20 recite limitations that are substantially equivalent to those of Claim 1, and are thus rejected under similar reasoning as applied to Claim 1 above.

5. In reference to Claim 4, Brooks discloses the limitations as applied to Claim 1 above. Brooks further discloses that said master interface is further configured to receive an early burst request signal from said master device before said first clock edge, said control logic is further configured to register said early burst request signal with said system clock to generate a burst request signal, and said slave interface is further configured to present said burst request signal to said slave device said delay after said first clock edge (See Column 1 Line 63 – Column 2 Line 7 and Column 4 Table 1 'HBURST').

6. Claim 16 recites limitations that are substantially equivalent to those of Claim 4, and thus is rejected under similar reasoning as applied to Claim 4 above.

7. In reference to Claim 5, Brooks discloses the limitations as applied to Claim 1 above. Brooks further discloses that said master interface is further configured to receive a bus request signal from said master device (See Column 6 Table 2 'HBUSREQx') and present a bus grant signal to said master device (See Column 6 Table 2 'HGRANTx'), and said control logic is further configured to arbitrate in response to said bus request signal and generate said bus grant signal (See Column 2 Lines 61-67 and Column 5 Lines 1-4).

8. Claim 17 recites limitations that are substantially equivalent to those of Claim 5, and thus is rejected under similar reasoning as applied to Claim 5 above.

9. In reference to Claim 6, Brooks discloses the limitations as applied to Claim 5 above. Brooks further discloses that said control logic is further configured to complete arbitration within one clock cycle of said system clock and present said command signal in a next clock cycle of said system clock (See Figure 7 'HWRITE' and 'PWRITE').

10. Claim 18 recites limitations that are substantially equivalent to those of Claim 6, and thus is rejected under similar reasoning as applied to Claim 6 above.

11. In reference to Claim 7, Brooks discloses the limitations as applied to Claim 5 above. Brooks further discloses that said master interface is further configured to receive a lock signal from said master device, and said control logic is further configured to halt arbitration responsive to said lock signal (See Column 6 Table 2 'HLOCKx').

12. Claim 19 recites limitations that are substantially equivalent to those of Claim 7, and thus is rejected under similar reasoning as applied to Claim 7 above.

13. In reference to Claim 8, Brooks discloses the limitations as applied to Claim 1 above. Brooks further discloses that said control logic comprises an address decoder configured to generate a plurality of device select signals responsive to an address signal (See Figure 8 'PSEL [1:n]' and Column 2 Lines 33-37).

14. In reference to Claim 9, Brooks discloses the limitations as applied to Claim 8 above. The bridge of Brooks will inherently include registers for storing, and subsequently transmitting, signals being transferred across the bridge.

15. In reference to Claim 10, Brooks discloses the limitations as applied to Claim 9 above. Brooks further discloses that said control logic further comprises an arbitration logic configured to generate a bus grant signal (See Column 2 Lines 61-67 and Column 5 Lines 1-4).

16. In reference to Claim 11, Brooks discloses the limitations as applied to Claim 10 above. Brooks discloses reliance upon the AMBA Specification (See Column 1 Lines 16-22). AMBA discloses a first multiplexor for multiplexing command signals responsive to a bus grant signal (See Page 3-4 Figure 3-2 'Address and control mux').

17. In reference to Claim 12, Brooks and AMBA disclose the limitations as applied to Claim 11 above. AMBA further teaches a second multiplexor for multiplexing write data select signals responsive to a bus grant signal (See Page 3-4 Figure 3-2 'Write data mux').

18. Claims 1, 13, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,339,395 to Pickett et al. ("Pickett").

19. In reference to Claim 1, Pickett discloses a bus comprising: a master interface (See Figure 1 Number 10) connectable to a master device external to said bus (See Figure 1 Number 12) and configured to receive an early command signal from said master device at a first clock edge of a system clock (See Figure 1 Number 18) and present a bus wait signal to said master device proximate a second clock edge of said system clock (See Figure 7 'DSACKL'); a slave interface (See Figure 1 Number 10) connectable to a slave device external to said bus (See Figure 1 Number 14) and configured to present a command signal to said slave device a delay after said first clock edge (See Figure 1 Number 26) and receive a slave wait signal from said slave

device (See Figure 7 'BUSY'); and a control logic configured to register said early command signal with said system clock to generate said command signal (See Figure 2 Number 52) and convert said slave wait signal into said bus wait signal (See Figure 7 Number 318).

20. Claims 13 and 20 recite limitations that are substantially equivalent to those of Claim 1, and are thus rejected under similar reasoning as applied to Claim 1 above.

21. Claims 1, 13, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,878,239 to Furuta ("Furuta").

22. In reference to Claim 1, Furuta discloses a bus comprising: a master interface (See Figure 2 Number 15) connectable to a master device external to said bus (See Figure 1 Number 14) and configured to receive an early command signal from said master device at a first clock edge of a system clock (See Column 2 Lines 34-37) and present a bus wait signal to said master device proximate a second clock edge of said system clock (See Column 2 Lines 37-40); a slave interface (See Figure 2 Number 15) connectable to a slave device external to said bus (See Figure 2 Number 31) and configured to present a command signal to said slave device a delay after said first clock edge (See Column 2 Lines 34-37) and receive a slave wait signal from said slave device (See Column 2 Lines 37-40); and a control logic configured to register said early command signal with said system clock to generate said command signal (See Column

2 Lines 34-37) and convert said slave wait signal into said bus wait signal (See Column 2 Lines 37-40).

23. Claims 13 and 20 recite limitations that are substantially equivalent to those of Claim 1, and are thus rejected under similar reasoning as applied to Claim 1 above.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks as applied to Claims 1 and 13 above, and further in view of US Patent Number 6,526,518 to Catlin et al. ("Catlin").

26. In reference to Claim 2, Brooks teaches the limitations as applied to Claim 1 above. Brooks further teaches that said master interface is further configured to receive an address signal from said master device, said control logic is further configured to register said address signal with said system clock to generate an address signal and decode said address signal to generate a device select signal, and said slave interface

is further configured to present said address signal and said device select signal to said slave device said delay after said first clock edge (See Figure 7 and Column 2 Lines 33-37). Brooks does not teach that the address signal is an early address signal. Catlin teaches the use of early addresses (See Column 12 Lines 31-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Brooks using the early address signals of Catlin, resulting in the invention of Claim 2, in order to allow the use of RAM as interface circuitries, since early addressing allows enough time to access the correct locations in the RAM (See Column 12 Lines 35-42 of Catlin).

27. Claim 14 recites limitations that are substantially equivalent to those of Claim 2, and thus is rejected under similar reasoning as applied to Claim 2 above.

28. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks and Catlin as applied to Claims 2 and 14 above, and further in view of US Patent Number 5,412,662 to Honma et al. ("Honma").

29. In reference to Claim 3, Brooks and Catlin teach the limitations as applied to Claim 2 above. Brooks and Catlin do not teach that said master interface is further configured to receive a no-address signal from a master device before a first clock edge and said control logic is further configured to inhibit said device select signal in response to said no-address signal. Honma teaches receiving a signal, which is

equivalent to a no-address signal, that is used by control logic to inhibit a select signal (See Figure 5 Number 3A and Column 6 Lines 35-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Brooks and Catlin with the select signal inhibit signal of Honma, resulting in the invention of Claim 3, in order to prevent an overwrite of the data written to the currently selected device (See Column 6 Lines 48-62 of Honma).

30. Claim 15 recites limitations that are substantially equivalent to those of Claim 3, and thus is rejected under similar reasoning as applied to Claim 3 above.

Claim Objections

31. Claims 1-12 are objected to because of the following informalities: The word "before" appears to have been omitted following the word "device" in Line 5 of Claim 1. Appropriate correction is required.

Response to Arguments

32. Applicant's arguments with respect to Claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Duty to Disclose

33. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56. Applicant is advised to submit any information material to patentability in accordance with 37 CFR 1.97 and 1.98.

Conclusion

34. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 6,122,690 to Nannetti et al.; US Patent Number 6,601,126 to Zaidi et al.; US Patent Number 6,912,611 to Kotlowski et al.; and US Patent Number 6,353,867 to Qureshi et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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